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10/757,212	01/14/2004	Jimmie Earl DeWitt JR.	AUS920030553US1	6480

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EXAMINER	
SAVLA, ARPAN P	

ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 09/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/757,212	DEWITT ET AL.	
	Examiner	Art Unit	
	Arpan P. Savla	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/19/06, 6/23/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

This Office action is in response to Applicant's communication filed June 19, 2006 in response to the Office action dated March 13, 2006. Claims 1, 2, 4, 5, 8-10, 12, 16-18, 20, and 23 have been amended. Claims 1-23 are pending in this application.

ACKNOWLEDGMENT OF REFERENCES CITED BY APPLICANT

Information Disclosure Statement

1. As required by MPEP § 609(c), Applicant's submission of the Information Disclosure Statements dated June 19, 2006 and June 23, 2006 are acknowledged by Examiner and cited references have been considered in the examination of the claims now pending. As required by MPEP § 609 c(2), a copy of the PTOL-1449 initialed and dated by Examiner is attached to the instant Office action.

OBJECTIONS

Specification

2. In view of Applicant's amendment, the objections to the specification have been withdrawn.

REJECTIONS NOT BASED ON PRIOR ART

Claim Rejections - 35 USC § 101

3. In view of Applicant's amendment, the 101 rejections to **claims 9-16** have been withdrawn.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-2, 4, 8, 9-10, 12, 16-18, 20, and 23 are rejected under 35 U.S.C. 103(a) as being obvious over Pekarich et al. (U.S. Patent 6,549,998) in view of IBM Technical Disclosure, "Hardware Cycle Based Memory Residency," hereafter "IBMTD," and in further view of Burrows (U.S. Patent 5,887,159).

6. **As per claim 1**, Pekarich discloses a method in a data processing system for processing instructions, the method comprising:

receiving a threshold value and an identification of a plurality of addresses to be monitored during the execution of a computer program (col. 4, lines 61-63; col. 3, lines 7-12; col. 1, lines 32-42);

Pekarich does not expressly disclose associating hardware counters with the plurality of addresses;

executing the computer program and incrementing respective hardware counters when the plurality of addresses are accessed and a performance indicator associated with the plurality of addresses is encountered;

and performing an action in response to a determination that a predefined relationship between the threshold value and a combination of values obtained from the hardware counters is present.

IBMTD discloses associating hardware counters with the plurality of addresses (pg. 1, paragraph 3, lines 1-2); *It should be noted that each page is associated with a page frame table which is in turn associated with physical addresses.*

and performing an action in response to a determination that a predefined relationship between the threshold value and a combination of values obtained from the hardware counters is present (pg. 1, paragraph 5, lines 8-10). *It should be noted that "page given immediately to the application requesting it when LRU runs" is analogous to "performing an action", "the difference between the hardware counter and the PFT counter is greater than the threshold" is analogous to "a predefined relationship between the threshold value and a combination of values obtained from the hardware counters is present", and "the difference between the hardware counter and the PFT counter" is analogous to "combination of values obtained from the hardware counters."*

Pekarich and IBMTD are analogous art because they are from the same field of endeavor, that being memory management.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement IBMTD's PFT and hardware counters with Pekarich's address range table.

The motivation for doing so would have been to reduce the expense of operations by allowing more immediate and more cost-effective memory management

with the use of a hardware cycle counter and PFT cycle counter (IBMTD, pg. 1, paragraph 4, lines 5-7).

The combination of Pekarich/IBMTD does not expressly disclose executing the computer program and incrementing respective hardware counters when the plurality of addresses are accessed and a performance indicator associated with the plurality of addresses is encountered.

Burrows discloses executing the computer program and incrementing respective hardware counters when the plurality of addresses are accessed and a performance indicator associated with the plurality of addresses is encountered (col. 5, lines 13-17 and 31-34; Fig. 5, elements 520 and 540). *It should be noted that "hit field" is analogous to "hardware counter", a "hit" to an entry in the prediction table" is analogous to an "address access", and "best_hint field" is analogous to "performance indicator." It should also be noted that the entries in the prediction table are associated with instruction addresses (col. 2, lines 2-4).*

The combination of Pekarich/IBMTD and Burrows are analogous art because they are from the same field of endeavor, that being data processing systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Burrow's dynamic determination of hint field values within Pekarich/IBMTD's address range table.

The motivation for doing so would have been to measurably improve system performance by making code run faster (Burrows, col. 6, lines 16-20).

Therefore, it would have been obvious to combine Pekarich, IBMTD, and Burrows for the benefit of obtaining the invention as specified in claim 1.

7. **As per claim 2**, the combination of Pekarich/IBMTD/Burrows discloses arithmetically combining values of the hardware counters to generate a combined counter value (IBMTD, pg. 1, paragraph 5, line 8); *It should be noted that "the difference between the hardware counter and the PFT counter" is analogous to "arithmetically combining values of the counters to generate a combined value counter value."*

comparing the combined counter value to the threshold value (IBMTD, pg. 1, paragraph 5, lines 8-9);

and performing the action in response to a relationship between the combined counter value and the threshold value being present (IBMTD, pg. 1, paragraph 5, lines 9-10).

8. **As per claim 4**, the combination of Pekarich/IBMTD/Burrows discloses the steps of arithmetically combining values of the hardware counters, comparing the combined counter value, and performing the action are performed in response to incrementing a hardware counter (Pekarich, col. 5, lines 17-23). *It should be noted that arithmetically combining values of counters, comparing the combined counter value, and performing the action are all done during separate iterations. The counters must be incremented by either +1 or +2 for the each iteration to occur. Therefore, the counters must first be incremented for the arithmetically combining values of counters, comparing the combined counter value, and performing the action to occur.*

9. **As per claim 8**, the combination of Pekarich/IBMTD/Burrows discloses arithmetically combining values of the hardware counters includes combining values in accordance with a condition indicated by a performance monitoring application (IBMTD, pg. 1, paragraph 5, line 8); *It should be noted that IBMTD discloses subtracting (i.e. arithmetically combining) values of the "hardware" and "PFT" counters. It is inherently required that this subtraction function of the ALU (i.e. a condition) is indicated by commands from the CPU (i.e. a performance monitoring application).*

10. **As per claim 9**, the claim is rejected for the same reasons as cited in claim 1 above combined with Pekarich's disclosure of a computer program product in a computer readable recordable-type medium for processing instructions (Pekarich, Pekarich, col. 5, lines 47-55).

11. **As per claim 10**, the claim is rejected for the same reasons as cited in claim 2 above combined with Pekarich's disclosure of a computer program product in a computer readable recordable-type medium for processing instructions (Pekarich, col. 5, lines 47-55).

12. **As per claim 12**, the claim is rejected for the same reasons as cited in claim 4 above combined with Pekarich's disclosure of a computer program product in a computer readable recordable-type medium for processing instructions (Pekarich, col. 5, lines 47-55).

13. **As per claim 16**, the claim is rejected for the same reasons as cited in claim 8 above combined with Pekarich's disclosure of a computer program product in a

computer readable recordable-type medium for processing instructions (Pekarich, col. 5, lines 47-55).

14. **As per claim 17**, Pekarich discloses an apparatus for processing instructions comprising:

means for receiving a threshold value and an identification of a plurality of addresses to be monitored during the execution of a computer program (col. 4, lines 61-63; col. 3, lines 7-12; col. 1, lines 32-42); *It should be noted that pg. 21, lines 4-6 of Applicant's specification appear to define this means as a computer.*

Pekarich does not expressly disclose means for associating hardware counters with the plurality of addresses;

means for executing the computer program and incrementing respective hardware counters when the plurality of addresses are accessed and a performance indicator associated with the plurality of addresses is encountered;

and means for performing an action in response to a determination that a predefined relationship between the threshold value and a combination of values obtained from the hardware counters is present.

IBMTD discloses means for associating hardware counters with the plurality of addresses (pg. 1, paragraph 3, lines 1-2); *It should be noted that pg. 21, lines 4-6 of Applicant's specification appear to define this means as a computer. Also, please see the citation note for the similar limitation in claim 1 above.*

and means for performing an action in response to a determination that a predefined relationship between the threshold value and a combination of values

obtained from the hardware counters is present (pg. 1, paragraph 5, lines 8-10). *It should be noted that pg. 21, lines 4-6 of Applicant's specification appear to define this means as a computer. Also, please see the citation note for the similar limitation in claim 1 above.*

Pekarich and IBMTD are analogous art because they are from the same field of endeavor, that being memory management.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement IBMTD's PFT and hardware counters with Pekarich's address range table.

The motivation for doing so would have been to reduce the expense of operations by allowing more immediate and more cost-effective memory management with the use of a hardware cycle counter and PFT cycle counter (IBMTD, pg. 1, paragraph 4, lines 5-7).

The combination of Pekarich/IBMTD does not expressly disclose means for executing the computer program and incrementing respective hardware counters when the plurality of addresses are accessed and a performance indicator associated with the plurality of addresses is encountered.

Burrows discloses means for executing the computer program and incrementing respective hardware counters when the plurality of addresses are accessed and a performance indicator associated with the plurality of addresses is encountered (col. 5, lines 13-17 and 31-34; Fig. 5, elements 520 and 540). *It should be noted that pg. 21,*

lines 4-6 of Applicant's specification appear to define this means as a computer. Also, please see the citation note for the similar limitation in claim 1 above.

The combination of Pekarich/IBMTD and Burrows are analogous art because they are from the same field of endeavor, that being data processing systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Burrow's dynamic determination of hint field values within Pekarich/IBMTD's address range table.

The motivation for doing so would have been to measurably improve system performance by making code run faster (Burrows, col. 6, lines 16-20).

Therefore, it would have been obvious to combine Pekarich, IBMTD, and Burrows for the benefit of obtaining the invention as specified in claim 17.

15. **As per claim 18**, the combination of Pekarich/IBMTD/Burrows discloses means for arithmetically combining values of the hardware counters to generate a combined counter value (IBMTD, pg. 1, paragraph 5, line 8); *It should be noted that pg. 21, lines 4-6 of Applicant's specification appear to define this means as a computer. Also, please see the citation note for the similar limitation in claim 2 above.*

means for comparing the combined counter value to the threshold value (IBMTD, pg. 1, paragraph 5, lines 8-9); *It should be noted that pg. 21, lines 4-6 of Applicant's specification appear to define this means as a computer.*

and means for performing the action in response to a relationship between the combined counter value and the threshold value being present (IBMTD, pg. 1,

paragraph 5, lines 9-10). *It should be noted that pg. 21, lines 4-6 of Applicant's specification appear to define this means as a computer.*

16. **As per claim 20**, the combination of Pekarich/IBMTD/Burrows discloses means for arithmetically combining values of the hardware counters, means for comparing the combined counter value to the threshold value, and means for performing the action operate in response to incrementing a counter (Pekarich, col. 5, lines 17-23). *It should be noted that pg. 21, lines 4-6 of Applicant's specification appear to define this means as a computer. Also, please see the citation note for claim 4 above.*

17. **As per claim 23**, the combination of Pekarich/IBMTD/Burrows discloses means for arithmetically combining values of the hardware counters includes combining values in accordance with a condition indicated by a performance monitoring application (IBMTD, pg. 1, paragraph 5, line 8). *It should be noted that pg. 21, lines 4-6 of Applicant's specification appear to define this means as a computer. Also, please see the citation note for claim 8 above.*

18. Claims 3, 6, 11, 14, 19, and 21 are rejected under 35 U.S.C. 103(a) as being obvious over Pekarich in view of IBMTD and in further view of Burrows as applied to claims 1, 9, and 17 above, and in even further view of Levine et al. (U.S. Patent 5,797,019).

19. **As per claim 3**, the combination of Pekarich/IBMTD/Burrows disclose a relationship between the combined counter value and the threshold value (IBMTD, pg. 1, paragraph 5, lines 8-9).

The combination of Pekarich/IBMTD/Burrows does not expressly disclose generating an interrupt if the predetermined relationship between the combined counter value and the threshold value is present.

Levine discloses generating an interrupt if the predetermined relationship between the counter value and the threshold value is present (col. 11, lines 3-7).

The combination of Pekarich/IBMTD/Burrows and Levine are analogous art because they are from the same field of endeavor, that being processing systems with counters.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use Levine's threshold invoked interrupt with Pekarich/IBMTD/Burrows' combined counter value system.

The motivation for doing so would have been to gain the benefit of having the performance monitor facility readily suitable for use in identifying system performance problems through use of appropriate counter values (Levine, col. 11, lines 7-9).

Therefore, it would have been obvious to combine Pekarich/IBMTD/Burrows and Levine for the benefit of obtaining the invention as specified in claim 3.

20. **As per claim 6**, the combination of Pekarich/IBMTD/Burrows/Levine discloses sending the interrupt to an interrupt handler of a performance monitoring application, wherein the interrupt handler performs an operation based on receipt of the interrupt (Levine, col. 9, lines 30-42; Fig. 4, elements 50, 57, 71, 77, and 79). *It should be noted that "performance monitor (PM)" is analogous to "performance monitoring application"*

and that "interrupt handling routines" are analogous to "operation based on receipt of the interrupt."

21. **As per claim 11**, the claim is rejected for the same reasons as cited in claim 3 above combined with Pekarich's disclosure of a computer program product in a computer readable recordable-type medium for processing instructions (Pekarich, col. 5, lines 47-55).

22. **As per claim 14**, the claim is rejected for the same reasons as cited in claim 6 above combined with Pekarich's disclosure of a computer program product in a computer readable recordable-type medium for processing instructions (Pekarich, col. 5, lines 47-55).

23. **As per claim 19**, the combination of Pekarich/IBMTD/Burrows disclose a relationship between the combined counter value and the threshold value (IBMTD, pg. 1, paragraph 5, lines 8-9).

The combination of Pekarich/IBMTD/Burrows does not expressly disclose generating an interrupt if the predetermined relationship between the combined counter value and the threshold value is present.

Levine discloses generating an interrupt if the predetermined relationship between the counter value and the threshold value is present (col. 11, lines 3-7).

The combination of Pekarich/IBMTD/Burrows and Levine are analogous art because they are from the same field of endeavor, that being processing systems with counters.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use Levine's threshold invoked interrupt with Pekarich/IBMTD/Burrow's combined counter value system.

The motivation for doing so would have been to gain the benefit of having the performance monitor facility readily suitable for use in identifying system performance problems through use of appropriate counter values (Levine, col. 11, lines 7-9).

Therefore, it would have been obvious to combine Pekarich/IBMTD/Burrows and Levine for the benefit of obtaining the invention as specified in claim 19.

24. **As per claim 21**, the combination of Pekarich/IBMTD/Burrows/Levine discloses means for sending the interrupt to an interrupt handler of a performance monitoring application, wherein the interrupt handler performs an operation based on receipt of the interrupt (Levine, col. 9, lines 30-42; Fig. 4, elements 50, 57, 71, 77, and 79). *It should be noted that pg. 21, lines 4-6 of Applicant's specification appear to define this means as a computer. Also, please see the citation note for claim 6 above.*

25. Claims 7, 15, and 22 are rejected under 35 U.S.C. 103(a) as being obvious over Pekarich in view of IBMTD, in further view of Burrows, and in view even further of Levine as applied to claims 3, 11, and 19 above, and in even further view of Bartfai et al. (U.S. Patent Application Publication 2003/0101367).

26. **As per claim 7**, the combination of Pekarich/IBMTD/Burrows/Levine disclose all the limitations of claim 7 except the operation is at least one of generating a log entry in a performance monitoring application log and notifying a log daemon process of an event.

Bartfai discloses the operation is at least one of generating a log entry in a performance monitoring application log and notifying a log daemon process of an event (paragraph 0030, lines 42-45; paragraph 0007, lines 20-22; paragraph 0037, lines 9-14; Fig. 2, element 140). *It should be noted that "Fault Service Daemon" is analogous to "log daemon."*

The combination of Pekarich/IBMTD/Burrows/Levine and Bartfai are analogous art because they are from the same field of endeavor, that being interrupt handling.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Bartfai's interrupt logging within Pekarich/IBMTD/Burrows/Levine's interrupt handling system based on combined counter values.

The motivation for doing so would have been to provide a mechanism for a more complete analysis of adapter error causes (Bartfai, paragraph 00300, lines 46-47).

Therefore, it would have been obvious to combine Pekarich/IBMTD/Burrows/Levine and Bartfai for the benefit of obtaining the invention as specified in claim 7.

27. **As per claim 15**, the claim is rejected for the same reasons as cited in claim 7 above combined with Pekarich's disclosure of a computer program product in a computer readable recordable-type medium for processing instructions (Pekarich, col. 5, lines 47-55).

28. **As per claim 22**, the combination of Pekarich/IBMTD/Burrows/Levine disclose all the limitations of claim 22 except the operation is at least one of generating a log entry

in a performance monitoring application log and notifying a log daemon process of an event.

Bartfai discloses the operation is at least one of generating a log entry in a performance monitoring application log and notifying a log daemon process of an event (paragraph 0030, lines 42-45; paragraph 0007, lines 20-22; paragraph 0037, lines 9-14; Fig. 2, element 140). *It should be noted that "Fault Service Daemon" is analogous to "log daemon."*

The combination of Pekarich/IBMTD/Burrows/Levine and Bartfai are analogous art because they are from the same field of endeavor, that being interrupt handling.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Bartfai's interrupt logging within Pekarich/IBMTD/Burrows/Levine's interrupt handling system based on combined counter values.

The motivation for doing so would have been to provide a mechanism for a more complete analysis of adapter error causes (Bartfai, paragraph 00300, lines 46-47).

Therefore, it would have been obvious to combine Pekarich/IBMTD/Burrows/Levine and Bartfai for the benefit of obtaining the invention as specified in claim 22.

29. Claims 5 and 13 are rejected under 35 U.S.C. 103(a) as being obvious over Pekarich in view of IBMTD, and in further Burrows as applied to claims 1 and 9 above, and in even further view of Randall Hyde, "The Art of Assembly Language," hereafter "Hyde."

30. **As per claim 5**, the combination of Pekarich/IBMTD/Burrows disclose arithmetically combining values of the counters (IBMTD, pg. 1, paragraph 5, line 8), comparing the combined counter value (IBMTD, pg. 1, paragraph 5, lines 8-9), and performing the action (IBMTD, pg. 1, paragraph 5, lines 9-10).

The combination of Pekarich/IBMTD/Burrows does not expressly disclose arithmetically combining values of the counters, comparing the combined counter value, and performing the action are performed within microcode of a processor of the data processing system.

Hyde discloses microcode of a processor of a data processing system (pg. 247, section 4.5, 2nd paragraph, lines 2-4).

The combination of Pekarich/IBMTD/Burrows and Hyde are analogous art because they are from the same field of endeavor, that being computer system design.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Hyde's microcode within Pekarich/IBMTD/Burrows' combined counter value system.

The motivation for doing so would have been to make better reuse of existing silicon on a CPU by using microcode subroutines to implement many common operations (Hyde, pg. 248, section 4.5, 6th paragraph, lines 1-4). Another motivation for doing so would have been to let programmers create some very complex instructions that consist of several different operations, thus providing programmers (especially assembly language programmers) with the ability to do more work with fewer instructions in their programs. In theory, this lets them write faster programs since they

now execute half as many instructions, each doing twice the work of a simpler instruction set (Hyde, pg. 248, section 4.5, 7th paragraph, lines 1-4).

Therefore, it would have been obvious to combine Pekarich/IBMTD/Burrows and Hyde for the benefit of obtaining the invention as specified in claim 5.

31. **As per claim 13**, the claim is rejected for the same reasons as cited in claim 5 above combined with Pekarich's disclosure of a computer program product in a computer readable recordable-type medium for processing instructions (Pekarich, col. 5, lines 47-55).

Response to Arguments

32. Applicant's arguments with respect to **claims 1-23** have been considered but are moot in view of the new grounds of rejection.

33. With respect to Applicant's arguments in the third full paragraph of page 13 of the communication filed June 19, 2006 which states "Pekarich and IBMTD, taken alone or in combination, do not teach or suggest "arithmetically combining values of the hardware counters includes combining values in accordance with a condition indicated by a performance monitoring application" the Examiner respectfully disagrees. In the same paragraph the Applicant goes on to state that "Applicants are claiming that values of the hardware counters are arithmetically combined when a condition indicated by a performance monitoring application is met." The Examiner would like to note that the features upon which Applicant relies are not recited in the claims. Applicant is calling for the hardware counters to be arithmetically combined when a condition is met,

however, this is not consistent with the claim language of claims 8, 16, and 23. Nowhere in these claims does it call for a condition to be met. When taking the broadest reasonable interpretation of claims 8, 16, and 23 as stated it is clear that IBMTD sufficiently teaches wherein subtracting (i.e. arithmetically combining) values of the hardware counters includes combining values in accordance with the subtraction function of the ALU (i.e. a condition) indicated by commands from the CPU (i.e. a performance monitoring application).

Conclusion

STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by MPEP 707.70(i):

CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, **claims 1-23** have received a second action on the merits and are subject of a second action final.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arpan P. Savla whose telephone number is (571) 272-1077. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on (571) 272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Arpan Savla
Art Unit 2185
August 23, 2006

SANJIV SHAH
PRIMARY EXAMINER